Amendments to the Specification

Please substitute the paragraph beginning on page 1, line 7, with the following paragraph:

This application is a continuation of U.S. Patent Application No. 09/606,485, filed June 29, 2000, which claims the benefit of U.S. Provisional Patent Application No. 60/141,393, filed June 29, 1999, the contents of both of which is hereby incorporated by reference.

Please amend the following paragraphs/sections as follows.

Please amend the paragraph beginning on page 1, line 12, as follows:

Power ~~Sequencing~~ sequencing circuits play a key role in a number of applications which require a controlled application of power sources, such as computer systems, and the like. In an integrated circuit having interconnected circuitry that is powered by differing voltages, a power sequencing circuit might be used to control the application of power supply voltages to the various circuits in an orderly manner. In interconnected circuits that operate on differing voltages, the circuits operating at the lower voltages tend to be the more susceptible to damage. Alternatively, power sequencing circuits are advantageously designed to protect circuits by utilizing a circuit configuration that avoids the turn on of parasitic circuit elements that tend to damage integrated circuitry.

Please amend the paragraph beginning on page 2, line 4, as follows:

There is therefore provided in a present embodiment of the invention a circuit for applying power to mixed mode integrated circuits in a predefined sequence to a first circuit powered by a first voltage and a second circuit powered by a second voltage that is less than the first voltage and having the second voltage coupled to the first circuit. The circuit for applying power to mixed mode integrated circuits includes[[,]] a modified [[IO]] I/O cell of the second circuit. The modified [[IO]] I/O cell has a driver transistor including a back gate terminal, a gate terminal that is driven by the second circuit, a ~~source~~ drain terminal that is coupled to a first circuit signal, and a ~~drain~~ source terminal that is coupled to the second ~~power supply~~ voltage.

Please amend the paragraph beginning on page 2, line 16, as follows:

The circuit for applying power to mixed mode integrated circuits further includes[[,]] a controller circuit coupled to the first voltage and the second voltage supplied as controller circuit inputs. The controller circuit has a plurality of controller circuit outputs.

Please amend the paragraph beginning on page 2, line 21, as follows:

The circuit for applying power to mixed mode integrated circuits also includes[[,]] a back gate bias application circuit. The back gate bias application circuit has a plurality of inputs coupled to the plurality of controller circuit outputs, and an output coupled to the ~~backgate~~ back gate of the driver transistor ~~backgate~~ back gate terminal.

Please amend the paragraph beginning on page 4, line 4, as follows:

FIG. 1 is a schematic diagram illustrating possible parasitic current flow from higher voltage power supply V_{HIGH} to a lower voltage power supply V_{LOW} at power supply turn on. A trend in integrated circuit design is to operate integrated circuits at lower power supply voltages. Low voltage power supply operation is desirable to reduce power dissipation and to allow fast circuit technologies to operate without breakdown voltage problems. If power supplies of differing voltages are present in a circuit, these power supplies do not reach their final value of voltage at the same time when they are activated. Also, if circuits 102, 104 operate from different power supply voltages[[,]] V_{LOW}, V_{HIGH}, [[The]] the components within the circuit tend not to rise to their final operating voltage at the same time tending to cause an undesired current flow 106.

Please amend the paragraph beginning on page 4, line 30, as follows:

The two circuits, and thus the power supplies V_{HIGH} and V_{LOW}, are typically coupled electrically by one or more interfacial connections such as shown at 115. Often circuits that operate from different potentials are present to achieve a given [[an]] overall desired circuit function. It is sometimes desirable to mix the circuits operating from different power supplies if lower power consumption can be achieved by utilizing one or more available circuits that operate from lower power supply voltages. A situation where this would arise is in the use of pre-designed intellectual property ("IP") cores, where because of time or budget constraints it is desirable to use the circuit as it was designed, without modifying it to operate from a common power supply voltage.

Please amend the paragraph beginning on page 5, line 10, as follows:

Interfacial connections are typically achieved in integrated circuits through one or more pads 116. The pads are typically coupled to a pin or lead of [[in]] an integrated circuit package, or to a chip carrier, via a wire bond. Current flow path 106 to the lower voltage power supply from the high voltage power supply is typically through one or more parasitic diodes, such as D2, present in a transistor M1. The parasitic diodes tend to be inherent to the internal circuitry of an integrated circuit ("IC") 102 operating from the lower supply voltage V_{LOW}. A common path for current flow to the lower voltage power supply is through interface circuitry M1 present at an integrated circuit pin. For example, in digital circuitry, interfacial circuitry of this type is often utilized to mix different logic families such as TTL, LS and CMOS. Additionally, digital circuitry often incorporates open collector transistor outputs into the designs as interfacial circuitry to provide sufficient and adjustable drive levels to circuitry coupled to these outputs.

Please amend the paragraph beginning on page 6, line 17, as follows:

FIG. 2 is a schematic of an embodiment of a circuit that prevents the turn-on of the parasitic diode present in the transistor by an incoming signal from a circuit operating at a higher voltage level. The technique requires that a connection to the higher voltage 120 is available on the integrated circuit 102. The higher voltage V_{HIGH} is tied to a ~~backgate~~ back gate 103 of one or more of the interfacial driver transistors M1 that tend to be prone to parasitic turn on.

Please amend the paragraph beginning on page 6, line 25, as follows:

A ~~backgate~~ back gate connection refers to a gate connection that includes the entire substrate of the integrated circuit. When a ~~backgate~~ back gate has a higher potential, parasitic diodes D1 and D2 do not turn on, preventing a large current flow, that would otherwise tend to damage the ICs. In a typical integrated circuit, a gate contact is disposed as a metalized pattern on the surface of an IC directly above a channel region of a field effect transistor. Typically, there is an insulating layer between the gate contact and the channel region. A ~~backgate~~ back gate connection consists of adding a contact to the substrate of the integrated circuit, that is on the opposite side of the integrated circuit from the gate contact.

Please amend the paragraph beginning on page 7, line 5, as follows:

The coupling of a ~~backgate~~ back gate contact to the substrate is established through to an upper surface of the wafer upon which the circuit is disposed. The ~~backgate~~ back gate contact is coupled to the polysilicon substrate through a diffusion window disposed in the integrated circuit.

Please amend the paragraph beginning on page 8, line 10, as follows:

Circuit 102 is shown as having an I/O cell or interfacial circuit 122. Integrated circuits typically ~~interfacial~~ interface circuitry 122 at each I/O connection 116. The I/O cell is connected to external voltages V_{LOW}, V_{HIGH} and to one or more external signal connections, such as shown at 115. The external signal typically originates from another circuit 104 that is operating at the same or higher voltage. Voltages V_{LOW} and V_{HIGH} are supplied as supply voltage rails within the I/O cell.

Please amend the paragraph beginning on page 8, line 18, as follows:

As shown, an incoming signal 115 to the low voltage circuit 102 is coupled to a driver transistor M1 at its ~~source~~ drain. A ~~drain~~ source of M1 is coupled to a low power supply rail. A back gate of transistor M1 is coupled to the higher voltage power supply, V_{HIGH} at pin 120.

Please amend the paragraph beginning on page 8, line 23, as follows:

A parasitic diode D1 tends to be present between the ~~drain~~ source and the back gate of M1. A parasitic diode D2 also tends to be present between the back gate and ~~source~~ drain of M1. A gate of M1 is being driven by internal circuitry of the I/O cell. Although this circuit [[is]] tends to be more robust, as previously mentioned, severe damage tends to occur if the system power supply is activated first. In some applications, a need for power supply sequencing tends to be undesirable. It is desirable to provide over voltage protection as described in FIG. 2 and additional circuitry that provides independent sequencing of the power supplies.

Please amend the paragraph beginning on page 9, line 3, as follows:

FIG. 3 is a schematic of an embodiment of the invention that tends to provide independent sequencing of the power supplies and parasitic current flow. Power supply status is evaluated by a controller circuit 110 to generate a set of control signals B1, B2 utilized by the I/O circuitry (122 of FIG. 2) to sequence the power supplies without damaging the IP core. The circuit of FIG. 2 is modified by the addition of two transistors that function as switches[[,]] MB1, MB2 (shown collectively in FIG. 3 as back gate bias application circuit 105) and a controller circuit 110. Transistors MB1 and MB2 prevent the back gate of M1

from being connected to the supplier voltage system power supply before the system power supply is available at its full voltage. Transistors MB1 and MB2 are controlled via gate signals B1 and B2 that are supplied by controller circuit 110.

Please amend the paragraph beginning on page 9, line 16, as follows:

The ~~source~~ drain of driver transistor M1 is coupled to an I/O signal 115 (of FIG. 2) at a pad [[116]] 119. The ~~drain~~ source of M1 is coupled to the low voltage supply rail set at voltage V_{LOW}. The back gate of driver transistor M1 is coupled in common to the ~~sources~~ drains and back gates of transistors MB1 and MB2. The ~~drain~~ source of MB1 is coupled to the system power supply line set at a voltage value V_{LOW} at 118. Transistor MB2 is coupled to a chip power supply set at a value of V_{HIGH} at 120.

Please amend the paragraph beginning on page 10, line 5, as follows:

From the power supplies, reference voltages V1 and V2 are created as inputs coupled to the comparator 112 (also designated as U1 in FIG. 4). The comparator output is fed to a bias generator 114 that generates the gate signals B1 and B2. The relationship between voltages B1 and B2 is such that they allow either MB1 or MB2 to turn on, but do not allow MB1 and MB2 to turn on simultaneously. Note that in an embodiment, MB1 and MB2 may be on simultaneously for a small period of time when the power supply values are rising faster than B1 and B2 can correct MB1 and MB2. In the exemplary embodiment, momentary overlap is minimal and is not as destructive as the case where the power sequencing circuit is absent. To drive the control signals B1 and B2, the comparator 112 takes a reading based upon the state of each power supply. Comparator inputs are voltages V1 and V2.

Please amend the paragraph beginning on page 10, line 19, as follows:

Voltage V1 is generated when the lower voltage chip power supply begins to ramp up in voltage value. When the chip power supply begins to supply voltage to the circuit, a current source I[[,]] starts current conduction through a chain of diodes DS. The diode chain DS provides the voltage drop V1. Voltage V1 provides an indication of the chip power supply reaching a given level. Voltage V1 is coupled to a negative terminal of the comparator [[U1]] 112.

Please amend the paragraph beginning on page 10, line 27, as follows:

Voltage V2 is the output of the resistive divider comprising resistors R1 and R2. Voltage V2 is the reference voltage that sets a trip point which causes a comparator 112 output ~~of U1~~ to change state. Resistor R1 has a first terminal that is coupled to the ~~systems~~ system's power supply line and a second terminal that is coupled to a first terminal of R2 and the positive input of the comparator [[U1]] 112. The second terminal of R2 is coupled to ground. The output of the comparator [[U1]] 112 is coupled to a bias generator circuit 114. The bias generator circuit 114 has inputs including the comparator input, V_{HIGH} and V_{LOW}. Bias generator outputs are voltages B1 and B2.

Please amend the paragraph beginning on page 11, line 3, as follows:

~~The bias generator circuit 114 had inputs including the comparator input, V_{HIGH} and V_{LOW}. Bias generator outputs are voltages B1 and B2.~~

Please amend the paragraph beginning on page 11, line 6, as follows:

FIG. 5 is a graph of the relationship of the voltages used in the power sequencing circuit of FIG. 3. At turn on and prior to the comparator ([[U1]] 112 of FIG. 4) changing state 140, V_{LOW} is applied to the ~~backgate~~ back gate of a driver transistor (M1 of FIG. 3) in the interfacial circuit of the low voltage circuit (102 of FIG. 3). During time interval 140, the voltage on the gate of MB2 of FIG. 3 is close to V_{LOW}, turning off MB2 and preventing the rising voltage of V_{HIGH} from being applied to the ~~backgate~~ back gate of M1 (of FIG. 3). Also during the time interval 140, the voltage B1 applied to the gate of MB1 of FIG. 3 is close to or equal to zero volts coupling V_{LOW} to the ~~backgate~~ back gate of M1 of FIG. 3.

Please amend the paragraph beginning on page 11, line 22, as follows:

During time interval 142, the levels of B1 and B2 (of FIG. 3) change state causing V_{HIGH} to be applied to the ~~backgate~~ back gate of a driver transistor (M1 of FIG. 3) in the interfacial circuit of the low voltage circuit (102 of FIG. 3). During time interval 140, the voltage on the gate of MB2 of FIG. 3 is reduced to a level below V_{LOW}, turning on MB2 and applying V_{HIGH} to the ~~backgate~~ back gate of M1 (of FIG. 3). Also during the time interval 142, the voltage B1 applied to the gate of MB1 of FIG. 3 is rising as the voltage of V_{HIGH} rises causing transistor switch MB1 (of FIG. 3) to turn off decoupling V_{LOW} from the ~~backgate~~

back gate of M1 of FIG. 3. The voltage V_{HIGH} on the ~~backgate~~ back gate of M1 continues to rise as V_{HIGH} ramps up to its final value.

Please amend the paragraph beginning on page 12, line 3, as follows:

FIG. 6 is a schematic diagram of an embodiment of a bias generator circuit 114. The bias generator circuit 114 includes [[3]] three inverting circuits 130, 132, U2. The inverter circuits produce output[[s]] levels B1 and B2 in response to the comparator 112 (of FIG. 4) output and the power supply voltages V_{HIGH} and V_{LOW} that tend to change on power up of a system. Outputs B1 and B2 are as shown in FIG. 5 and control the application of V_{LOW} and V_{HIGH} to a ~~backgate~~ back gate of a driver transistor M1 (of FIG. 3) in an interfacial circuit.

Please amend the paragraph beginning on page 12, line 11, as follows:

Signals B1 and B2 do not function as conventional inverter signals that switch between power supply rails and ground. Inverter U2 is [[a]] conventionally constructed as known by those skilled in the art.

Please amend the paragraph beginning on page 13, line 3, as follows:

In the bias generator circuit 114, the inverter U2 is coupled to the V_{LOW} power supply. The inverter input terminal is coupled to the output terminal from the comparator ([[U1]] 112 of FIG. 4). The inverter output terminal is coupled to a gate of Q1.

Please amend the paragraph beginning on page 13, line 7, as follows:

A modified inverter for B2 logic levels 130 includes a PMOS transistor Q1 and [[PMOS]] NMOS transistors Q2, Q3, and Q4. Transistor Q1 includes a source terminal coupled to V_{LOW}, a ~~backgate~~ back gate terminal coupled to V_{LOW}, and a drain terminal coupled to output B2[[,]] and coupled to a drain terminal of Q2. A conventional current source I2 has [[a]] an input terminal coupled to V_{LOW}, and an output terminal coupled to the ~~source~~ drain of Q2.

Please amend the paragraph beginning on page 13, line 14, as follows:

Transistor Q2 includes a gate terminal coupled to B2, a ~~backgate~~ back gate terminal coupled to a ground, and a source terminal coupled to a drain terminal of Q3. Transistor Q3 includes a gate terminal coupled to the gate terminal of Q1, a ~~backgate~~ back gate terminal coupled to ground, and a source terminal coupled to a drain terminal of Q4. Transistor Q4 includes a gate terminal coupled to the drain terminal of Q3, a ~~backgate~~ back gate terminal coupled to ground, and a source terminal coupled to ground.

Please amend the paragraph beginning on page 13, line 22, as follows:

A modified inverter for B1 logic levels 132 includes a PMOS transistor Q5[[,]] and NMOS transistors Q6 and Q7. Transistor Q5 includes a source terminal coupled to V_{HIGH}, a gate terminal coupled to B2, a ~~backgate~~ back gate terminal coupled to V_{HIGH}, and a drain coupled to terminal B1.

Please amend the paragraph beginning on page 13, line 27, as follows:

Transistor Q6 includes a drain terminal coupled to terminal B1, a gate terminal coupled to the input of inverter U2, a ~~backgate~~ back gate terminal coupled to ground, and a source terminal coupled to a drain of Q7. Transistor Q7 includes a gate terminal coupled to the input of inverter U2, a ~~backgate~~ back gate terminal coupled to ground, and a source terminal coupled to ground.

Please amend the paragraph beginning on page 14, line 18, as follows:

IP cores 102, 104 are often interconnected so that an I/O connection exists between a first IP core 102, and a second IP core 104. IP core [[104]] 102 is biased by a voltage V_{LOW}, that is lower in value than the bias voltage applied to the second IP core, V_{HIGH}.

Please amend the paragraph beginning on page 14, line 30, as follows:

In the embodiment shown, several low voltage circuits or "cores" 102[[,]] are disposed on an integrated circuit substrate 108. In addition, one or more cores that operate at higher voltages 104 are present on the substrate and functionally interact with the low voltage circuits or "cores".